Add the following claims.

24. The transistor of claim 9 wherein said first source/drain region is a source region, said second source/drain region is a drain region and wherein said first V_T is higher than said second V_T.

25. The transistor of claim 10 wherein said first source/drain region is a source region and said second source/drain region is a drain region.

26. The transistor or claim 11 wherein said first source/drain region is a source region and said second source/drain region is a drain region.

REMARKS

Claims 9 to 11 have been amended, claims 15, 22 and 23 have been canceled without prejudice and claims 24 to 26 have been added. Accordingly, claims 9 to11 and 24 to 26 are now active in this application.

The specification has been amended to correct the errors kindly noted by the Examiner.

Claim 10 has been amended to overcome the rejection under 35 U.S.C. 112, second paragraph.

Claims 9 and 11 were rejected under 35 U.S.C. 102(b) as being anticipated by Sasaki (U.S. 4,371,955 B1). The rejection is respectfully traversed.

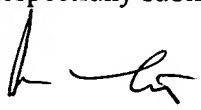
Claim 9 requires, among other features, a channel region having a first dopant profile contacting the first source/drain region to provide a first V_T and a second dopant profile different from the first dopant profile contacting the second source/drain region to provide a second V_T different from the first V_T. No such structure is taught or suggested by Sasaki either alone or in the total combination as claimed.

Claim 11 depends from claim 9 and therefore defines patentably over Sasaki for at least the reasons stated above with reference to claim 9.

Claim 11 further limits claim 9 by requiring that the first dopant profile be a relatively low V_T dopant implant and the second dopant profile be a selective relatively high V_T dopant implant. No such structure is taught or suggested by Sasaki either alone or in the combinatin as claimed.

Claims 24 to 26 depend from claims 9 to 11, claim 10 apparently being allowable, and therefore define patentably over Sasaki for at least the reasons set forth as to claims 9 and 11 above as to claims 24 and 26, claim 25 depending from an apparently allowable claim and therefore also being allowable.

Respectfully submitted,



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B1 [0011] FIGURES 3A to 3C show steps in the process flow in accordance with a third embodiment of the present invention;

B2 [0016] It should be understood that the V_T of region 17 is a result of the combination of what has been referred to as the high V_T and the low V_T implant. One can be a counter-doping of the other. The result is an effective channel length, L, which is independent of the original disposable gate length. Fabrication then proceeds in standard manner to complete the device.

B3 [0017] As a second embodiment, the low V_T channel implant can be performed prior to the high V_T implant. After removal of the disposable gate, disposable sidewalls are formed on the mask as in FIGURE 1B of the first embodiment and as shown in FIGURE 2A wherein like reference characters refer to the same or similar structure. The sidewall on the source region side 11 is retained and the sidewall on the drain region side 13 is removed with appropriate deposition and patterning of resist and etching in standard manner. A low V_T region 21 is then provided by implant of the channel as shown in FIGURE 2B. The remaining sidewall 11 at the source end of the channel is then removed and a high V_T implant is implanted into the channel region between the source and drain regions. Preferably, the high V_T implant is of opposite conductivity type to the low V_T implant to provide a high V_T region 23 and a low V_T region 21. Fabrication then proceeds in standard manner to complete the device. Optionally, the high V_T implant can be performed prior to formation of the sidewalls.

[0018] As a third embodiment, it is desirable to add a liner 25 over the mask surface, sidewalls and pad oxide prior to fabrication as noted above with reference to the first and/or second embodiments and particularly over the structure as shown in FIGURE 1A and the structure as shown in FIGURE 2A prior to formation of the sidewalls 11, 13 with subsequent formation of the sidewalls 11, 13 over the liner as shown in FIGURE 3B. The liner 25 is preferably silicon nitride. Fabrication then proceeds as in the prior embodiments as discussed above.

[0019] As a fourth embodiment as shown if FIGURES 4A and 4B, the FET can be made in a symmetrical rather than asymmetrical embodiment as described in the first and second embodiments with a different implant 27 in the center of the channel region as shown in FIGURE 4A. Optionally, implant 27 may include a punch-through implant. The sidewalls 11, 13 are then removed and the entire channel region is doped wither n- or p-type to provide either a less heavily net doped region adjacent the source and drain regions 3, 5 if the same conductivity type dopant is used or a more heavily net doped region adjacent the source and drain regions if the opposite conductivity type dopant is used and the opposite characteristic in region 27 as shown in FIGURE 4B. Optionally, the implant in the full channel region can be performed prior to sidewall formation. Fabrication then proceeds in standard manner to complete the device.

9. A transistor which comprises:

(a) a semiconductor substrate having a surface and having a first source/drain region and a second source/drain region spaced apart from each other and extending to said surface; and

(b) a channel region disposed in said substrate between said first and second source/drain regions in said substrate and extending to said surface, said channel region having a first dopant profile contacting said first source/drain region to provide a first V_T and a second dopant profile different from said first dopant profile contacting said second source/drain region to provide a second V_T different from said first V_T.

10. A transistor which comprises:

(a) a semiconductor substrate having source and drain regions therein; and

(b) a channel region between said source and drain regions in said substrate having a relatively low V_T central region between said source and drain regions and relatively high V_T regions adjacent to said source and drain regions;

wherein said channel region is an implanted low V_T dopant intermediate said source and drain regions and an implanted high V_T dopant adjacent said source and drain regions.

11. The transistor of claim 9 wherein said first dopant profile is a relatively low V_T dopant implant and said second dopant profile is a selective relatively high V_T dopant implant.

24. The transistor of claim 9 wherein said first source/drain region is a source region, said second source/drain region is a drain region and wherein said first V_T is higher than said second V_T.

25. The transistor of claim 10 wherein said first source/drain region is a source region and said second source/drain region is a drain region.

26. The transistor or claim 11 wherein said first source/drain region is a source region and said second source/drain region is a drain region.